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Low Power and High Performance MTCMOS Conditional Discharge Flip Flop

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Abstract: Power consumption in high performance integrated circuits have been one of the most serious constraints in designs recently. The conditional discharge flip flop(CDFF) belonging to one of the fastest pulse triggered flipflop reduces internal switching activities as that of existing explicit pulse triggered Data close to output flipflop (Ep-DCO). Registers are the main parts for processing information eg: in counters, accumulators etc.,. Implementation of these registers using CDFF can achieve low power consumption and high performance. MTCMOS (multi threshold CMOS) technique saves the leakage power during standby mode operations and hence, enhances the circuit performance for long battery life applications. We find that, using both MTCMOS and conditional discharge technique in flip flop, improves the performance and also consumes low power. In this paper, we simulate CDFF and the proposed MTCMOS CDFF to prove that MTCMOS CDFF is the best among the fastest pulse triggered flipflops. We also implement an application 4 bit shift register using proposed MTCMOS conditional discharge flip flop.

Keywords: Conditional Discharge Flip Flop (CDFF), Explicit Pulsed Data Close to Output Flip Flop (ep-DCO), MTCMOS Technique.

INTRODUCTION

Mostly power consumption in dynamic flip-flops occurs due to the internal node switching activities. These switching because of the precharge and discharge paths being opened during the input and output state changes. Many techniques were proposed to reduce these internal node switching activities [1]. They are conditional precharge, conditional capture and conditional discharge techniques [2]. As compared to all the three techniques, conditional discharge technique is the most efficient and complexity of the circuit is less. In this paper we implement two types of double edge triggered, explicit pulsed flip-flops namely,

1. Explicit pulsed data close to output flipflop
2. Conditional discharge flipflop.

The comparison is also done. In both the flip-flops explicit pulse triggering allows us for double edge triggering and also power sharing among multiple flip flops. The clock switching activity is hence reduced.

In section II, we explain the concept of ep-DCO flip flop. In section III, we explain the concept of CDFF with and without MTCMOS technique is communicated. In part IV, we discuss simulation outcomes and comparisons ep-DCO and CDFF flip flops. In section V, implementation of 4 bit shift registers using CDFF and its power comparison with and without MTCMOS. Section V follows conclusion.

EXPLICIT PULSE TRIGGERED FLIPFLOP

One illustration of explicit pulse brought on flip-flop (ep-FF) is the express pulsed data close to output (ep-DCO) Flip-flop; it's considered probably the fastest flip-flops as a result of its semi-dynamic constitution. It's right fitted to very excessive-overall performance features[3], in which it is able to be employed within the maximum important paths of a design to attain an awfully small flip-flop enlarge. This makes it viable for extra freedom in cycle budgeting in particular with its horrible setup time feature this is

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because of using the heart beat triggering mechanism. Fig. 1 is the schematic for the ep-DCO flip-flop; its semi-dynamic charter consists of levels: a dynamic (first stage) and a static stage (second).

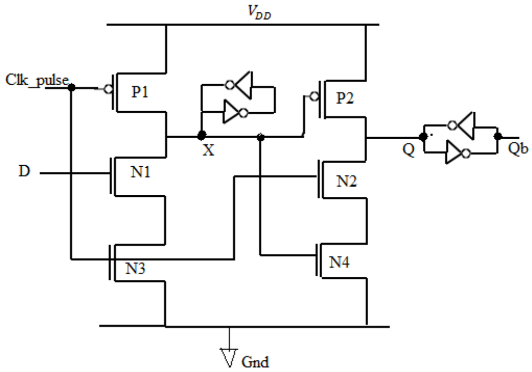

Fig. 1: Double edge triggered explicit-pulsed flipflop (ep-DCO flipflop)

Principle of Operation of Explicit Pulsed Data Close to Output (ep-DCO) Flipflop

From Fig. 1, we find that on the rising fringe of the clock transistors N2 and N3 activate for a short interval of time, which is the same as the extend incurred through the heartbeat generator. For the duration of this interval, the flip flop is obvious and the input information propagates to the output. After the transparent period, the pull- down paths in each level is turned off via the equal transistors N2 and N3. The double edge triggering clock pulse is generated and given as input to the clocked transistors P1, N2, and N3 by a pulse generator as shown in Fig. 2.

Thus any alternate on the enter aren't capable of go to the output. Keepers are used to preserve the output and inner node states whilst the circuit is inside the maintain mode. Cautious evaluation of the ep-DCO circuit famous an enormous quantity of energy being consumed by way of charging and discharging the indoors node X through P1 transistor which does at every clock cycle, substantially while the input D will not be changing. Additionally, whilst the output is excessive, the repeated charging/discharging of node X in each clock cycle factors system faults to expose up on the output. These machine faults propagate to the pushed gates now not handiest to broaden their switching vigor intake however also to motive noise troubles so one can cause system mal-functioning.

CONDITIONAL DISCHARGE FLIP FLOP

The flip-flop structure used right here is identical as the express pulsed knowledge just about output (ep-DCO) semi dynamic structure. The schematic diagram of the proposed conditional discharge flip-flop (CDFF) is shown in Fig. Three. It uses a pulse generator as shown in Fig. 2. For double edge triggering or sampling. The flip-flop is made from two levels. Stage one is accountable for shooting the low-to-high transition. Stage two is responsible for capturing high-to-low transition.

Principle of Operation of Conditional Discharge Flipflop (CDFF)

When D input switches from low to high, initially X is precharged to Vdd and output (Q, Qb) are (low, high). When D is at high transistor N1, N3, N5 transistors are on and X discharges through N1, N3, and N5 to ground. Then Output Q charges to Vdd through P2. The Transistor N4 is OFF and output Q stays high as long as D input stays high. Internal node X is again recharged to V_{DD} as discharge path at dynamic stage shuts off by the Qb. When D input switches from high to low, as D goes for high to low transition, the transistor N4 is ON due to Y becomes high. The discharge path is ON and output Q is discharged to ground through N2 and N4. Thus output Q captures high to low transition. X remains in its precharged state as N1 turns off due to D input.

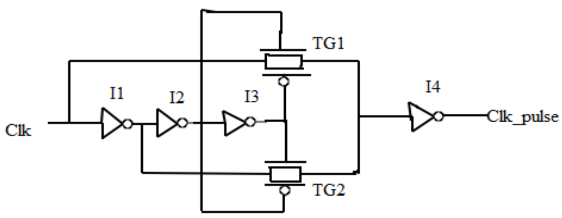

Fig. 2: Clock pulse generator used for Double edge triggering

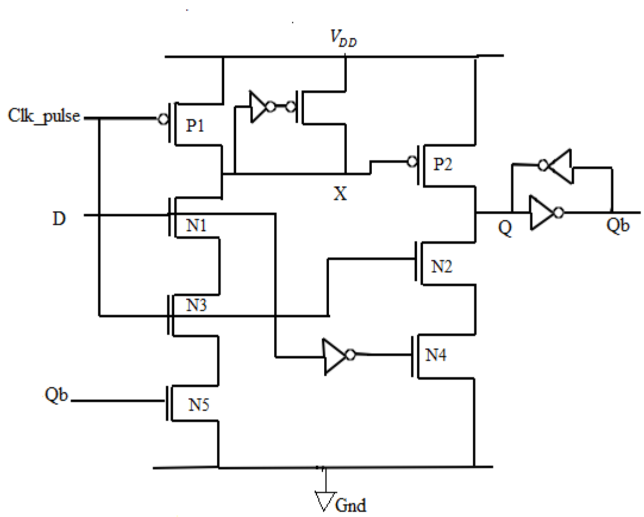

Fig. 3: Conditional Discharge Double-edge triggered Flipflop

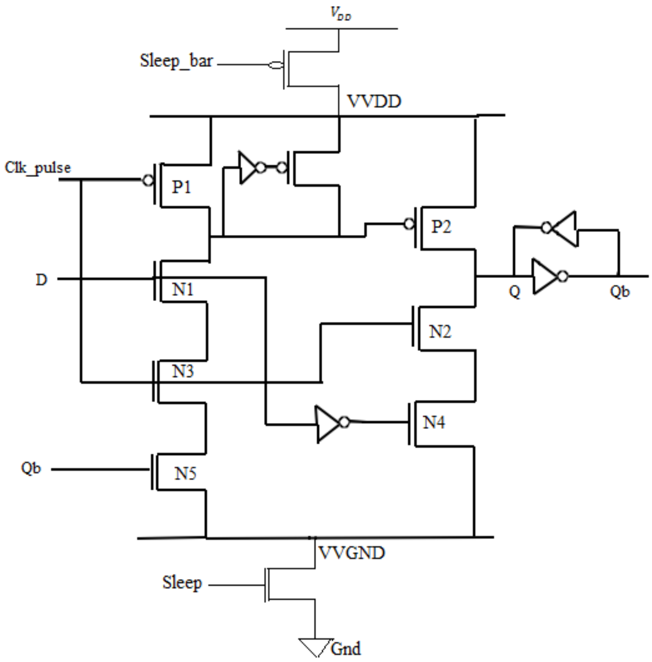

Fig. 4: Conditional Discharge Flipflop with MTCMOS technique

Due to the fact that node X shouldn't be discharged and charged each clock cycle, no glitches appear on the output node Q when the input D stays excessive, and Q will not be discharged at the establishing of every valuation. For that reason, CDFF elements much less switching noise new release. Additionally, node X stays excessive or recharged quite often, which helps in shortening the keeper constitution as shown in Fig. 3. Additionally, clock gating may also be with ease applied to do away with power consumption when input D keeps the identical value. This conditional discharge flip flop can be modified using MTCMOS (multi threshold CMOS) technique [2] as shown in Fig. 4 for reducing the standby power. The transistors with thin lines are the sleep transistors. These sleep transistors are used in the MTCMOS technique for reducing the sub threshold leakage currents when the circuit is not in use. These sleep transistors can be controlled for further reducing the standby power i.e., when input and output are in same state and the circuit can be disabled by using the sleep signals. The transistors other than sleep transistors are given low threshold voltage, for high speed operation. The sleep transistors are to be sized optimally to overcome delay and area penalties. We chose threshold voltages for high v_{th} transistors are 0.6V and -0.6V and for low v_{th} transistors as 0.3V and -0.32V for NMOS and PMOS respectively.

COMPARISON OF EP-DCO AND CDFF

The simulation outcome for all Flip-flops have been bought in a 0.18μm CMOS science at room temperature making use of HSPICE, the give voltage is 1.Eight V. A clock frequency of 125 MHz is used alternatively of 250 MHz used in single part triggered Flip-flops.

The upward push time and fall time of the clock are stored at 100ps. C_{Load} for both the flip-flops are kept at 22.08fF. The C_{Load} is the load of 4 cascade flip-flops used for constructing a 4-bit register. It has been observed that in fig 7, the output wave form ep-DCO flip flop lot of switching activities at node X exists when D is stable High. This is due to the simultaneous precharging and discharging of node X at every clock cycle. Also some glitches appear at the output Q. These glitches increases power consumption of the circuit. In Fig. 9 we observe the output wave form of MTCMOS CDFF which is also same as CDFF with reduced glitches as compared to ep-DCO flip flop at node Q because of reduced internal switching activities at node X. As the discharge path is controlled by the output Qb in CDFF which avoids the simultaneous charging and discharging of internal node X. It is observed that Power consumption is abridged as evaluated to ep-DCO flip flop as glitches at the output Q are reduced when D input stays High.

Power Consumption Comparison of Ep-DCO and CDFF

In table I, we compare total average power consumed including the clock pulse generator power by the explicit pulsed data close to output flip flop (ep-DCO) and the conditional discharge flipflop. Conditional discharge Flip flop achieves low power and high performance with less energy consumption and high speed. The ep-DCO consumes more power dissipation is because of the glitches in the output. And also, CDFF with MTCMOS technique achieves power delay product approximately equal to CDFF. So, it's better to use MTCMOS technique for reducing stand by leakage power consumption.

Table I: Power and delay comparison of flip flops

Flip flop	Delay	Total average power consumed	Power Delay product
Ep-DCO	216ps	80.67μw	17.280fJ
CDFF	223ps	77.199μw	17.17fJ
MTCMOS CDFF	236ps	71.49μw	16.7fJ

From the fig 6, from the chart it is observed that even though the delay of the MTCMOS CDFF is increasing the increase in the power delay product curve is below the CDFF and EPDCO flip-flops curves. Thus this shows that MTCMOS CDFF is the best in achieving low power and also high performance.

BIT SHIFT REGISTER IMPLEMENTATION USING MTCMOS CDFF

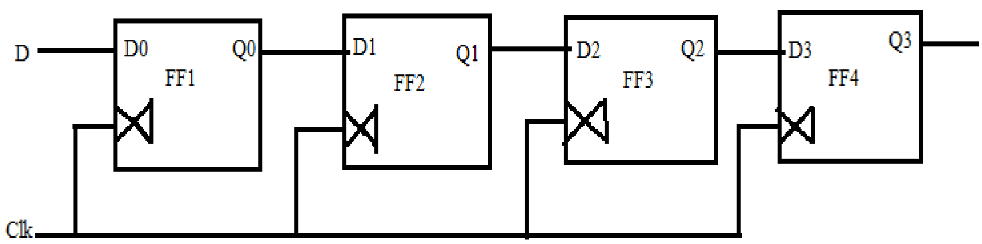

Fig. 5: 4 bit shift register implementation using proposed flip flops

Fig. 5 is the implementation of 4 bit shift register implementation using double edge triggered conditional discharge flip flop (CDFF). This can also be implemented using proposed MTCMOS CDFF. One set of sleep transistors (PMOS and NMOS) are enough for all the flip-flops in the four bit register to control the circuit instead of placing sleep transistors separately for each and every CDFF. In this way we can save the area. Table II is the power consumption comparison of CDFF with and without MTCMOS technique. It is observed that usage of MTCMOS CDFF saves 18% of power consumed as that of conventional CDFF.

Table II: Comparison of 4bit shift register

Type	Total average power consumed at 250MHz
Ep-DCO	165μw
CDFF	152.17μw
CDFF(MTCMOS)	128.18μw

The power compared also includes the clock pulse generator power which is shared among the flip flops. In Fig. 10 we observe the shift operation of data of a 4 bit shift register using MTMCOS CDFF. This four bit shift register can be used to implement a low power and high performance linear feedback shift register (LFSR) for cryptography and is also valuable as evaluated to gray and binary counter and diversity of other applications.

CONCLUSION

In this manuscript, MTCMOS technique is introduced in conditional discharge flip-flop to reduce the internal node switching activities and also the leakage power. While ep-DCO is appropriate for critical paths, CDFF is appropriate for both speed insensitive paths and speed- critical paths for power efficiency. In terms of Power Delay Product, ep-DCO CDFF outperforms, Conditional Precharge Flip flops and conditional capture. The CDFF with MTCMOS technique is the best to use in registers and counter applications.

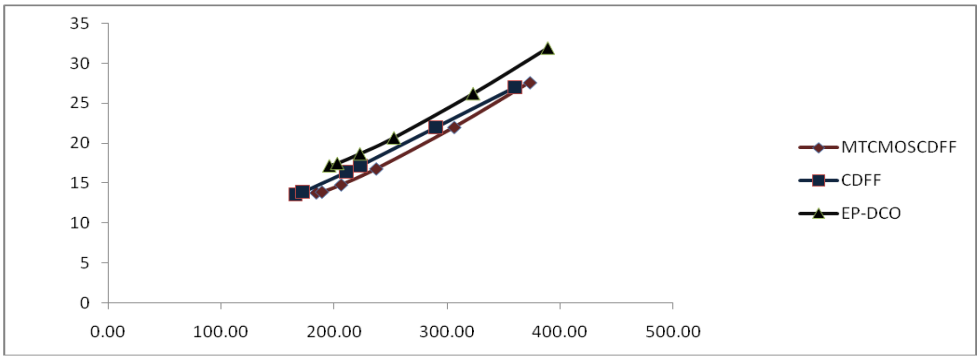

Fig. 6: Hspice simulated output wave forms of CDFF flip flop

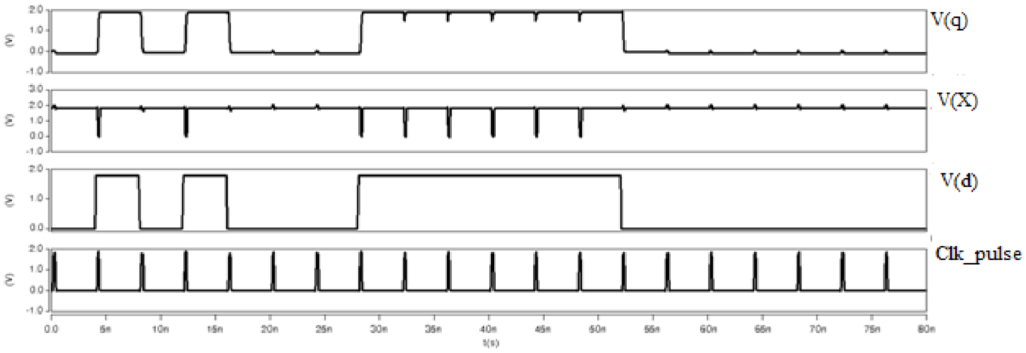

Fig. 7: Hspice simulated output wave form of EP-DCO flip flop

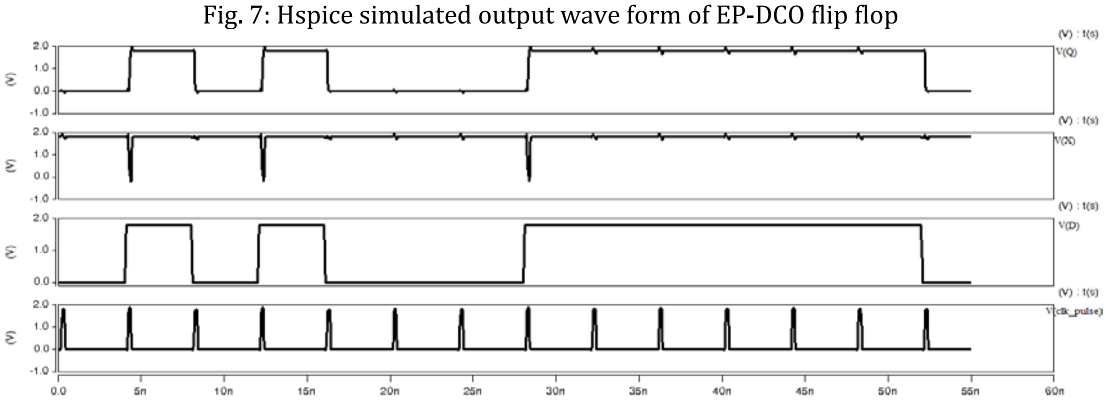

Fig. 8: Hspice simulated output wave form of CDFF flip flop

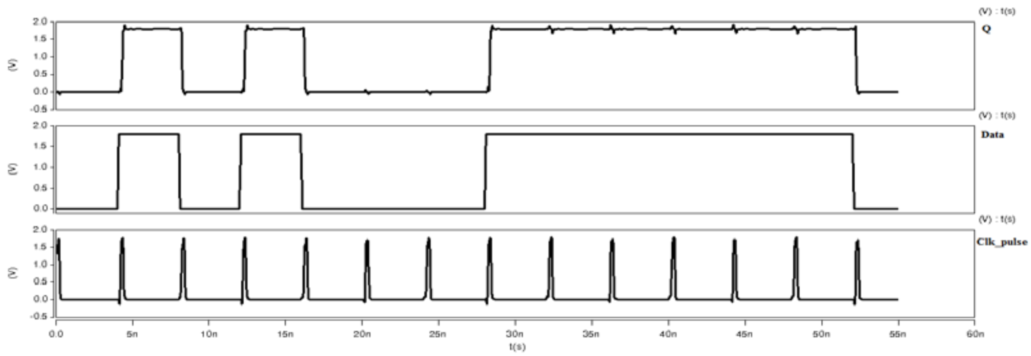

Fig. 9: Hspice simulated output wave form of MTCMOS CDFF flip flop

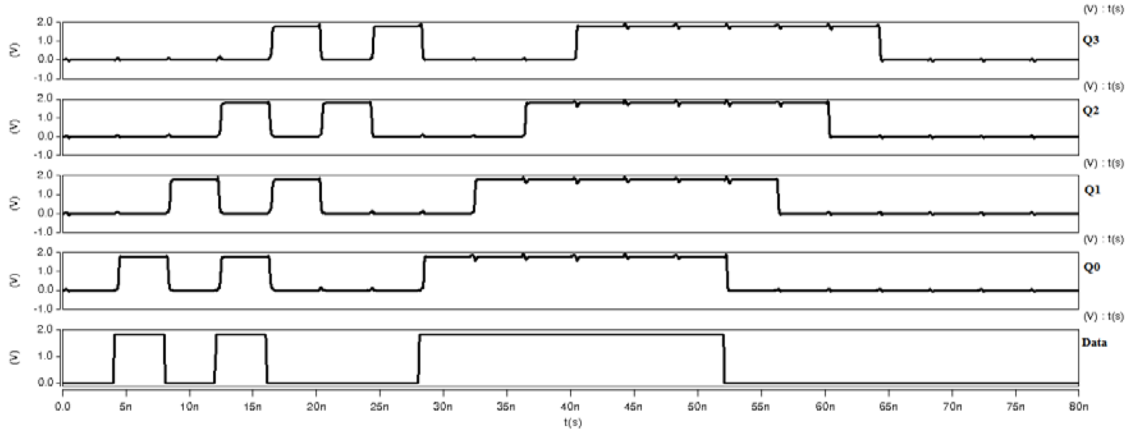

Fig. 10: 4 bit shift register output of MTCMOS CDFF flip flop

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